Optimized pulse width modulation strategy for reduced switch multilevel inverters

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Abstract

In the energy conversion process, the quality of the power supply can be obtained through a multilevel inverter. These inverters produce the AC output voltages in terms of multi-level. The gating signal generated is directly related to harmonics. This work reports a novel pulse width modulation strategy developed the pulses to on and off the power semiconductor switches of multilevel inverter. An effort made to get better performance of multilevel inverter and reduce significant lower order harmonic energies by using the modified hybrid carrier with trapezoidal reference based pulse width modulation strategy. The comprehensive harmonic analysis of the output of various modulation indices and the results compared with a Sinusoidal PWM strategy. This proposed PWM strategy has implemented in real time through FPGA Xilinx Spartan 3 system. The simulation and experimental results reveal the lowest harmonic distortion and highest output RMS voltage.

Keywords: *Distortion factor, Harmonic distortion, Modified Hybrid Carrier Pulse Width Modulation, Multilevel Inverter.*

1. Introduction

Multilevel inverters increase in industrial applications as a choice of power conversion. These inverters are generating the output voltage in terms of many steps by synthesizing DC voltages. Due to this, switching stress minimized, total harmonic distortion reduced and increased RMS voltage (fundamental) compared to the conventional inverter. Even though plenty of merits available, there is a drawback associated with the number of components and corresponding gate signals. These twin problems are rectified through minimizing the power semiconductor components and providing proper gate signals. Rodriguez et al [1] made a detailed survey about different topologies and analyzed the various controlling strategies like sinusoidal pulse width modulation, selective harmonic elimination and space-vector modulation. Hongyan Wang et al [2] demonstrates the new PWM strategies based on control freedom degree combinations to get higher RMS voltage with less harmonic distortion. The different control techniques for cascaded multilevel inverter presented in [3]. Chaturvedi et al [4] describe a variety of control strategies for five level diode clamped multilevel inverter. Bendre et al [5] designed three level diode clamped inverter using a multicarrier for obtaining voltage regulation. Multi carrier based pulse width modulation strategies have been analyzed based on output voltage of the inverter subsequent novel multi carrier modulation technique is proposed in the literature [6]. Aghdam et al [7] proposed various carriers based PWM strategies for an asymmetrical multilevel inverter. Fei et al [8]

discussed the problems which are associated with sub harmonic PWM strategies and proposed novel method for obtaining switching angle. Tengfei Wang [9] analyzed multicarrier PWM techniques through applying in the cascaded multilevel inverter. In literature [10] trapezoidal amalgamated reference proposed for a cascaded multilevel inverter with unipolar PWM strategy. This new reference enhances the overall performances of the inverter. The total harmonic distortion and output voltage of cascaded multilevel inverter controlled by carrier pulse width modulation techniques
have been reported in the literature [11]. Soumitra Das and Narayanan [12] proposed alternative switching sequences for a Three-Level Inverter and the harmonic distortion is studied and compared with the conventional space vector pulse width modulation strategy. Obrad Dordevic et al [13] made a comparison of carrier-based strategies with space vector strategies, implementing three level inverter fed induction motor drive. Jose Ignacio Leon et al [14] introduces a modulation technique based on multidimensional for H-bridge multilevel inverters. A new carrier based pulse width modulation strategy implemented in diode clamped multilevel inverter in the literature [15]. In recent decays, multilevel inverter with reduced switch dominates the traditional DCMLI, FCMLI and cascaded H-bridge MLI due to flexibility in the gate signal generation and complexity. Many of researchers proposed multilevel inverter with reduced switches has been reported in various literature [16, 17]. Hsieh et al [18] proposed seven level inverter and discussed the switching losses and voltage stress of the inverter. Gandhi raj et al [19] proposed push-pull multilevel inverter and their corresponding gate pulses are developed through a field programmable gate array based controller. Perez Ramirez et al [20] proposed a novel modulation strategy consisting of the combinations of the staircase and PWM switching combinations to enhance the lower distortion in output AC voltages. A detailed survey analysis of multilevel inverter topologies in terms of binary and trinary along with various modulation strategies in the literature [21].

From the above discussion, the carrier based pulse width modulation strategy is the most excellent and flexible control. Many kinds of literature focusing on the pulse width modulation strategy with the triangular carrier signal. To obtain the least total harmonic distortion and higher DC bus utilization, carriers are altered by various shapes along with different frequencies. These carriers are continually compared with the trapezoidal reference. In these works, the chosen reduced switch multilevel inverter is triggered by the above strategies.

2. Multilevel Inverter Topology

The new modified structural design consists of three DC sources with identical voltage magnitude, six switches, and one diode. The additional level can be achieved by inserting one DC source along with one switch. The switch count of the proposed topology is half the switch count of the cascaded H-bridge topology. Figure.1 represents the proposed topology.

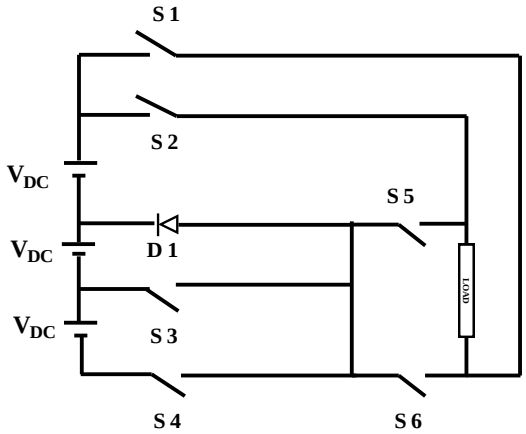

Figure 1 Reduced switch multilevel inverter

The voltage levels generated by the inverter are $3V_{DC}$, $2V_{DC}$, V_{DC}, 0, $-V_{DC}$, $-2V_{DC}$, $-3V_{DC}$. The output voltage levels at different switching states are represented in Table.1

Table 1 Switching states of Reduced switch multilevel inverter

Switching States						Output Voltage V_o
S_1	S_2	S_3	S_4	S_5	S_6	
0	1	0	1	0	1	$3V_{DC}$
0	1	1	0	0	1	$2V_{DC}$
0	1	0	0	0	1	V_{DC}
1	1	0	0	0	0	0
1	0	0	0	1	0	$-V_{DC}$
1	0	1	0	1	0	$-2V_{DC}$
1	0	0	1	1	0	$-3V_{DC}$

The conduction in positive and negative half cycles takes place by S_2, S_6, and S_1, S_5 respectively. In both the half cycles, the switches S_3 and S_4 generate the intermediate and outermost voltage levels. The diode D_1 is responsible for generating the initial voltage levels in both the half cycles.

3 Modified Hybrid Carrier PWM Strategy (MHCPWM)

In conventional sub harmonic PWM strategy, triangular carrier with fixed amplitude and fixed frequency are compared with the sinusoidal reference signal. The modulation strategy classified as unipolar and bipolar. In the the bipolar scheme for an m level inverter, m-1 carriers needed to generate pulses. A variety of carrier pattern drastically reduces the total harmonic reduction compared with conventional strategies reported in the literature [22]. Many research papers focused on the harmonic reduction and they are compromised in RMS output voltage. This work reports a novel strategy developed by the amalgamation of various carrier signals triangular, trapezoidal, rectified sine and sawtooth along with different frequencies and identical amplitudes. To achieve lower harmonic distortion and high RMS output voltage, these signals are compared with the trapezoidal signal. The modulation index m_a is

$$m_a = \frac{2A_m}{(m-1)A_c}$$

Where
A_m - Amplitude of reference signal
A_c - Amplitude of carrier signal

This technique can be easily expanded to any level. The conventional Sinusoidal Pulse Width Modulation (SPWM) which includes a constant triangle as a carrier and sine as a reference also used to trigger the gates and both the results are compared. In addition to the above, based on vertical disposition PWM strategies are classified as

3.1 Modified Hybrid Carrier PWM Strategy – I (MHCPWM - I)

In this method, six carriers were placed above and below zero reference line and all the carriers are in the same phase. Carrier and reference wave arrangements are as shown in Figure 2

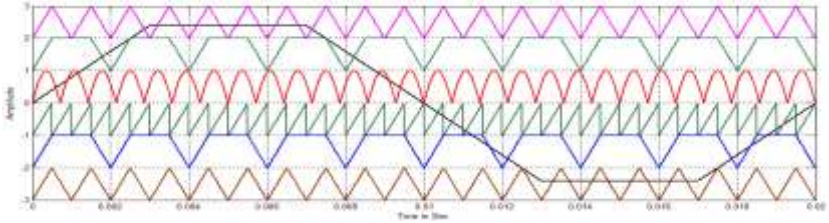

Figure 2 Carrier arrangement for MHCPWM - I strategy with trapezoidal reference

3.2 Modified Hybrid Carrier PWM Strategy – II (MHCPWM - II)

This technique consists, the carriers having a variable amplitude and the same frequency was placed above the zero reference are in phase and below the zero reference. The carriers placed above and below were 180-degree phase shifted with respect to the above reference.

3.3 Modified Hybrid Carrier PWM Strategy – III (MHCPWM - III)

The carriers having a variable amplitude and the same frequency was placed above the zero reference are in phase and below the zero reference. The carriers placed above and below were 180-degree phase shifted with respect to the above reference.

For all the above strategies, switching pattern is shown in Figure 3

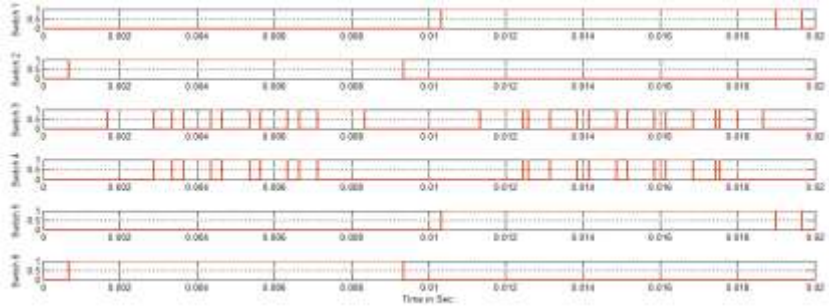

Figure 3 Switching pattern

In this article, the following performance parameters are considered for analyzing the inverter

Harmonic factor (HF_n)

$$HF_n = \frac{V_{on}}{V_1} \; for \; n > 1 \qquad (1)$$

Where, V_{on} - RMS value of n[th] harmonic component

V_1 - fundamental component

Total Harmonic Distortion (THD)

$$\mathrm{THD} = 1/\mathrm{V}_1 \left\{ \sqrt{\sum_{n=2,3}^{\infty} \mathrm{V_{on}}^2} \right\} \qquad (2)$$

Distortion Factor (DF)

$$\mathrm{DF} = 1/\mathrm{V}_1 \left\{ \sqrt{\sum_{n=2,3}^{\infty} \left(V_{on}/n^2 \right)^2} \right\} \qquad (3)$$

4 Simulation Results

The single phase reduced switch multilevel inverter was modeled using MATLAB/SIMULINK using a power system block set. Simulations were carried out for different values of modulation indices. Figure 4 & 5 shows the simulated output voltage generated by the SPWM strategy and their corresponding Fast Fourier Transform (FFT) plot. Figure 6 & 7 shows the simulated output voltage generated by the MHCPWM - I strategy and their corresponding FFT plot. Figure 8 & 9 shows the FFT spectrum of MHCPWM - II and MHCPWM - III strategies. The corresponding values of %THD and V_{RMS} are measured using their values are shown in Tab 2 and 3 respectively. % DF for the chosen strategies is calculated using their values is shown in Tab 4. Figure 10 and 11 shows the %THD and V_{RMS} comparison chart. The following parameter values are used for MATLAB simulation: R-L load = 100 ohms, 0.5mH, V_{DC} =100V.

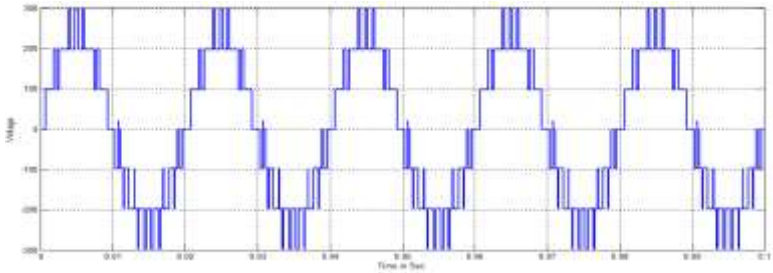

Figure 4 Output voltage generated by SPWM Strategy

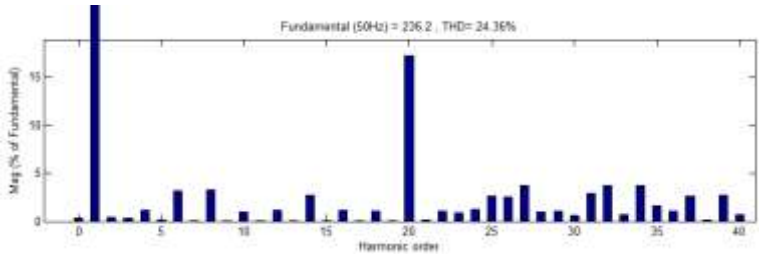

Figure 5 FFT plot for output voltage of SPWM Strategy

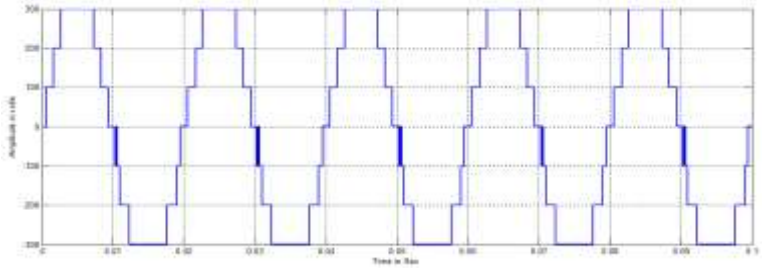

Figure 6 Output voltage generated by MHCPWM - I strategy with Trapezoidal Ref

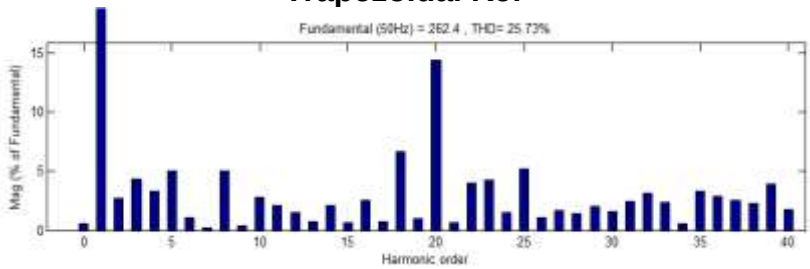

Figure 7 FFT plot for output voltage of MHCPWM - I strategy with Trapezoidal Ref

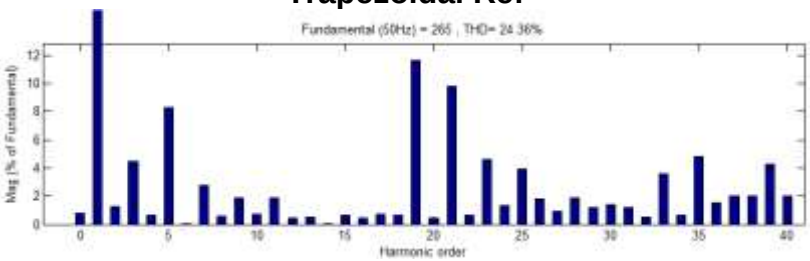

Figure 8 FFT plot for output voltage of MHCPWM - II strategy with Trapezoidal Ref

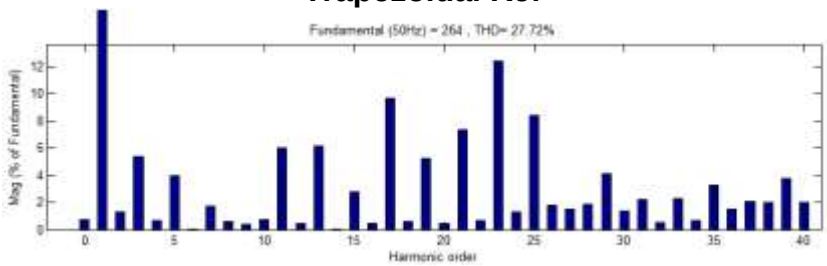

Figure 9 FFT plot for output voltage of MHCPWM - III strategy with Trapezoidal Ref

Table 2 % THD comparison for different Modulation Strategy

m_a	MHCPWM I	MHCPWM II	MHCPWM III	SPWM
1	13.03	12.27	15.03	18.39
0.9	22.87	20.75	24.19	22.67
0.8	25.73	24.36	27.72	24.36

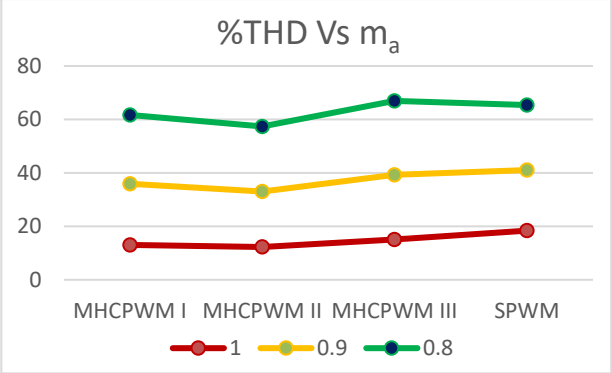

Figure 10 %THD Vs Modulation Strategies

Table 3 V_{RMS} comparison for different modulation Strategy

m_a	MHCPWM I	MHCPWM II	MHCPWM III	SPWM
1	234.1	226.9	234.6	209.6
0.9	209.4	207.2	210.5	188.2
0.8	185.5	187.4	186.7	167.1

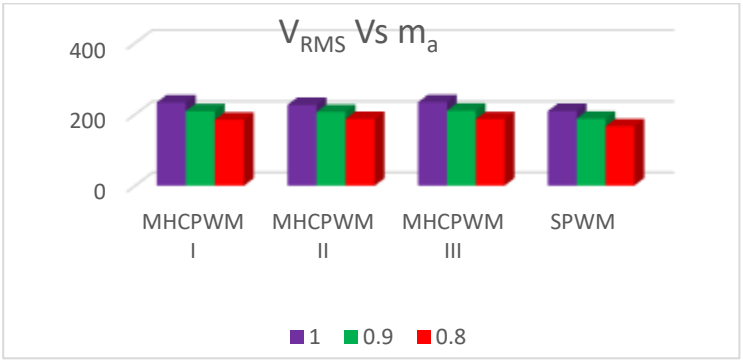

Figure 11 V_{RMS} Vs Modulation Strategies

Table 4 % Distortion Factor for different modulation Strategy

m_a	MHCPWM I	MHCPWM II	MHCPWM III	SPWM
1	0.8783	0.2405	0.3225	0.0164
0.9	0.9718	0.2002	0.5513	0.0169
0.8	1.123	0.3676	0.8028	0.0173

The following information acquired from the simulation results:

It is observed from Fig 5, 7, 8 and 9 that the harmonic distortion of the output voltages is lesser in MHCPWM – II and higher V_{RMS} in MHCPWM - III. The MHCPWM – I strategies also closer in V_{RMS}. In continuation of the above

- From Tab 2 and Fig 10 it is inferred that MHCPWM - II strategy offers lower harmonic distortion.
- Tab 3 and Fig 11 show MHCPWM - III strategy provides higher DC bus utilization.
- 20^{th} harmonic energies appear in both SPWM and MHCPWM - I strategies.
- 19^{th} harmonic energies dominant in MHCPWM - I strategies.
- 19^{th} & 21^{st} harmonic energies appear in MHCPWM - II strategies.

- 17^{th} and 21^{st} harmonic energies appear in MHCPWM - III strategy.

5 Experimental Results

To enhance the superiority of the proposed modulation strategies, the experimental setup of the seven-level inverter has been developed using Xilink SPARTAN based FPGA system. Real-time implementation of these strategies using an FPGA system requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/SIMULINK. The FPGA system combines a data acquisition system with an independent processing system to execute digital control. It is a real-time control system based on SPARTAN XCS3S100E floating-point processor with four channel 8 bit analog to digital converter (ADC), single channel DAC, four 18 * 18 pipelined hardware multipliers and four 18K bit block RAMs running at 200 MHz. The FPGA system can be plugged into a PCI slot of a PC. The gate signal generated through simulations targeted into the FPGA system by JTAG emulator. Optocoupler circuit provides separation between the control circuit and the power converter circuit. The peak-to-peak output voltage is limited to 12V due to laboratory constraints. The experimental results are viewed in digital storage oscilloscope and their harmonic analyses are obtained through the power quality analyzer. Fig 12 shows the entire prototype setup. The best strategies obtained from simulations, TAR reference based strategies are implemented in the hardware model, which results are shown only for one sample value of modulation index value 0.8. Figs 13 to 18 displays the output voltages and its corresponding harmonic spectrum of symmetrical seven-level inverter obtained using MHCPWM - I, MHCPWM - II and MHCPWM - III strategies with trapezoidal reference respectively. Tab 5 shows the comparison of %THD and of an output voltage with different PWM strategies for various values of modulation index. The V_{RMS} of fundamental output voltage for different modulation indices is listed in Tab 6. The following parameter values are used for experimentation: V_{DC} =12V, R-L (load) = 100Ω, 0.5mH, fc=1000Hz and fm=50Hz.

Figure 12 Hardware Setup

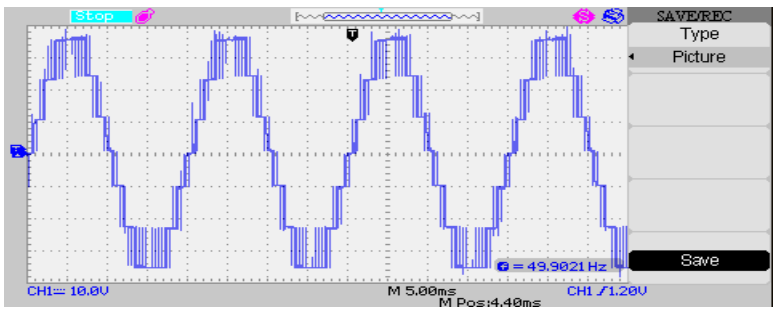

Figure 13 Hardware Output voltage by MHCPWM - I strategy

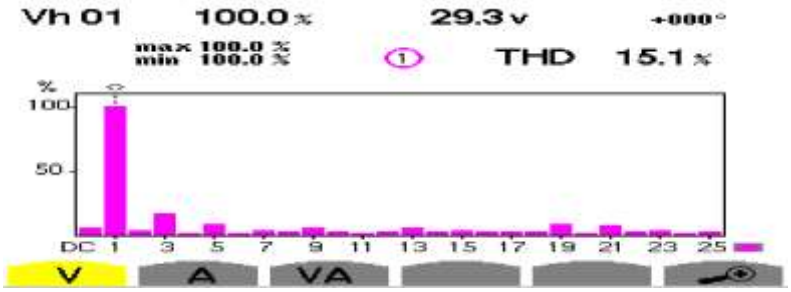

Figure 14 FFT plot of MHCPWM - I strategy

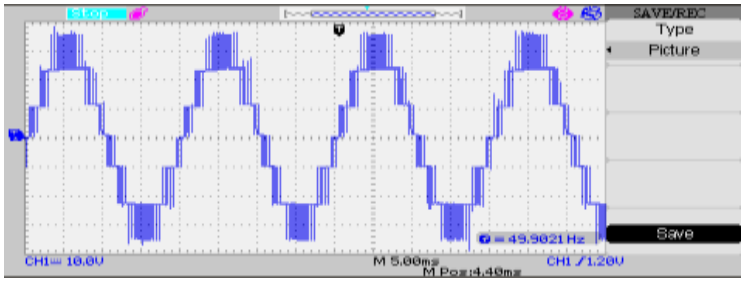

Figure 15 Hardware Output voltage by MHCPWM - II strategy

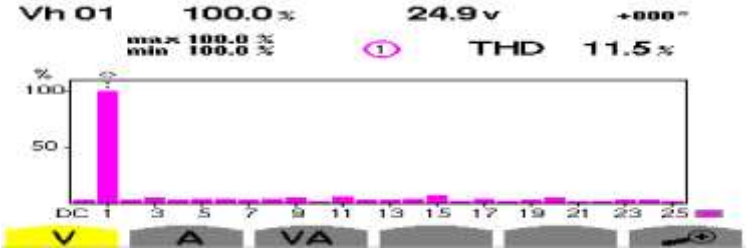

Figure 16 FFT plot of MHCPWM - II strategy

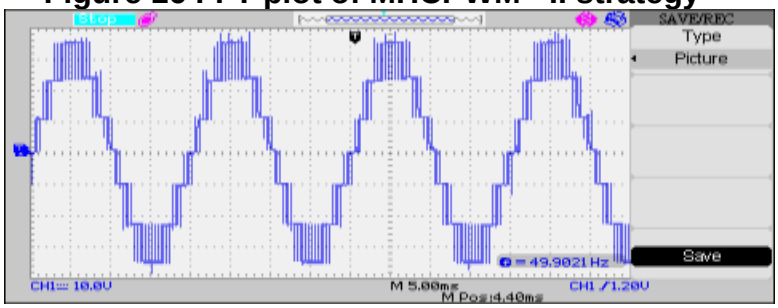

Figure 17 Hardware Output voltage by MHCPWM - III strategy

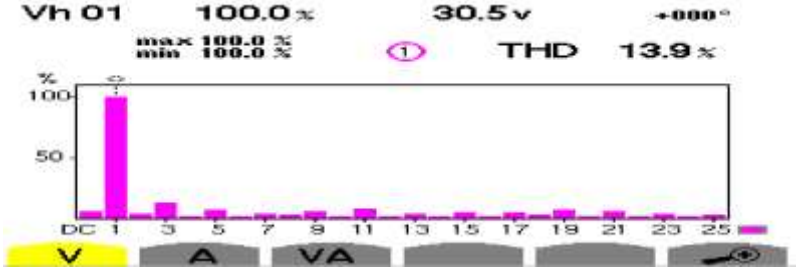

Figure 18 FFT plot of MHCPWM - III strategy

Table 5 THD for different modulation indices

m_a	MHCPWM I	MHCPWM II	MHCPWM III
1	11.4	9.5	11.8
0.9	12.8	10.9	12.9
0.8	15.1	11.5	13.9

Table 6. V_{RMS} for different modulation indices

m_a	MHCPWM I	MHCPWM II	MHCPWM III
1	33.5	29.4	35.2
0.9	31.5	26.5	32.4
0.8	29.3	24.9	30.5

6 Conclusion

The modified hybrid PWM strategy has been developed and simulated for various modulation indices ranging from 0.8-1 for the reduced switch multilevel inverter and then implemented in real time using FPGA. The results are revealed to each other.

The performance parameters like (i) THD showing purity of the output voltage, (ii) V_{RMS} (fundamental) indicating the amount of DC bus utilization and (iii) DF indicates the amount of harmonics that remains in the output voltage after its second order attenuation linked to power quality issues have been tabulated and analyzed.

It is found that the MHCPWM - II strategy provides relatively lower %THD and MHCPWM - III shows higher DC bus utilization (fundamental) and lower % distortion factor. The SPWM strategy exhibits a lower distortion factor compared modified hybrid PWM strategy**.**

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